CLAIMS

What is claimed is:

1. A memory device, comprising:

a memory array for storing at least one data bit and configured to electrically operate from a power supply voltage; and

a circuit configured to receive an external reference voltage and generate in response thereto an internal reference voltage independent of said power supply voltage, said internal reference voltage for accessing and evaluating said at least one data bit in said memory array.

2. The memory device of claim 1, further comprising data input/output circuitry coupled to said memory array and further coupled and responsive to said internal reference voltage of said circuit.

3. The memory device of claim 1, further comprising an address register coupled and responsive to said internal reference voltage of said circuit.

4. The memory device of claim 1, wherein said internal reference voltage generated by said circuit tracks said external reference voltage.

5. The memory device of claim 1, wherein said circuit comprises a following circuit configured to generate an internal reference voltage that is dependent upon an external reference voltage.

6. The memory device of claim 1, wherein said circuit comprises a voltage follower configured to receive said external reference signal at an input and configured to generate in response thereto said internal reference signal.

7. The memory device of claim 1, wherein said circuit comprises a plurality of voltage followers serially coupled to receive an external reference voltage and generate in response thereto an internal reference voltage.

8. The memory device of claim 1, further comprising circuitry for configuring said memory device as one of a DRAM, SDRAM, Rambus memory, double data rate memory and flash memory.